REMARKS

By the present amendment, a new title has been submitted and the Abstract has been amended to improve its presentation. Entry of these amendments is respectfully requested.

In the Office Action, the examiner has made a number of minor objections to the application as set forth in the following identified by paragraph number:

2. The drawings contain Japanese characters. Accompanying this Amendment is a Letter re Drawings where proposed drawing changes to delete Japanese characters has been made. Since the drawings also contain a translation of the Japanese characters, the proposed drawing correction only involves deletion of the characters;

3. The title is not descriptive. The title has been amended to read as the examiner suggested;

4. The claims must start on a separate page. The specification has been amended such that the claims start on a separate page; and

5. The abstract should not contain claim terminology such as "means." The Abstract has been amended herein to delete the claim terminology.

Accordingly, withdrawal of the objection to the specification is respectfully requested.

Claims 1-5 were rejected under 35 USC § 103(a) as being unpatentable over the patent to Maruyama in view of the patent to Glenn et al. In making this rejection, it was asserted that the patent to Maruyama teaches the basic method as claimed except for the steps of marking the semiconductor device. The patent to Glenn et al was then asserted to supply these teaching deficiencies regarding marking. Reconsideration of this rejection in view of the following comments is respectfully requested.

With regard to this rejection, it is to be noted that the patent to Maruyama is assigned to the same assignee as the subject application (Fujitsu Limited) and that both applications were copending. A recent amendment to 35 USC § 103(c) became effective as to any application filed after November 29, 1999. This amendment provides that prior art effective under the provisions of 35 USC § 102(e), that is, a U.S. patent having a filing date prior to the filing date of the subject application, is no longer effective prior art if the two have the same assignee. Since the Maruyama patent and the subject application are assigned to the same assignee and the basis for citation of the Maruyama patent is 35 USC § 102(e) as the patent issued after the filing date of the subject application, the above provisions of § 103(c) apply and the prior art rejection has been obviated.

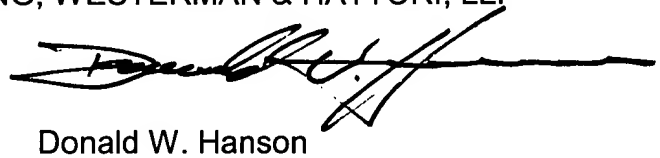
For the reasons stated above, withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claim 1 through 5 over the cited patents are respectfully requested.

In view of the foregoing, it is submitted that the subject application is now in condition for allowance and early notice to that effect is earnestly solicited.

In the event this paper is not timely filed, the undersigned hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 01-2340, along with any other additional fees which may be required with respect to this paper.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



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PATENT TRADEMARK OFFICE

Marked Up Version of Amendments to Specification and Claims

IN THE SPECIFICATION:

Amend the specification as follows:

(Page 1, lines 2-3): MANUFACTURE OF WAFER LEVEL SEMICONDUCTOR DEVICE ~~AND SEMICONDUCTOR DEVICE~~ WITH QUALITY MARKINGS ON THE SEALING RESIN

(Page 13, lines 1-26):

thereafter attach the resin sheet having the marking to the rear surface of the wafer.

Thereby, the marking information including the position information and result of electrical test is not required to temporarily print unlike the first embodiment and the result of electrical test can be marked on the resin sheet simultaneously when the test is performed.

Moreover, it is also possible to previously print the numerals and codes indicating the position information of the chip on the resin sheet and then attaching the resin sheet to the rear surface of wafer under the condition of Fig.2(a). In this case, the result of electrical test is not printed. The result of electrical test is no longer required to print on the resin sheet in the case where such result is stored in the memory together with the position information of chip. Thereby, the marking process of the test result may be omitted and accordingly the processes may be saved.

[Effect of the Invention]

As explained above, according to the method of manufacturing wafer level semiconductor device of the present invention, sine the information indicating where the internal chips are located on the wafer can be printed on the diced semiconductor package, the trace-ability of search for defective product can be very much improved.

~~What is claimed is:~~

~~1. A method of manufacturing wafer level semiconductor device, comprising the steps of:~~

(Page 14, lines 1-26):

What is claimed is:

1. A method of manufacturing wafer level semiconductor device, comprising the steps of:

sealing the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on the front surface with resin material;

a first marking the position information corresponding to each chip in the region of each chip at the rear surface of said wafer;

conducting electrical test to each chip;

a second marking the result of said electrical test corresponding to each chip in the region of each chip at the rear surface of said wafer; and

dicing the wafer into each chip.

2. A method of manufacturing wafer level semiconductor device comprising:

sealing the front surface of a wafer having the front and rear surfaces and having formed a plurality of semiconductor chips on the front surface thereof with resin material;

conducting electrical test to each chip;

marking in the region of each chip at the rear surface of said wafer, the position information corresponding to each chip and the result of said electrical test; and

dicing the wafer into each chip.

3. A method of manufacturing wafer level semiconductor as claimed in claim 1 or 2, wherein the circuit surface of said wafer and the opposite surface thereof are sealed with resin material and said position information and result of electrical test are marked in the region of each chip on the surface.

IN THE ABSTRACT:

(Page 17, lines 2-17):

~~The object of the present invention is to provide a~~ A method of manufacturing semiconductor device in the method of manufacturing wafer level semiconductor device that can search the defective products from the marking information even when sealing resin is formed on the wafer and a semiconductor device manufactured with the same method. ~~The means for solving the object is a~~ A method of manufacturing wafer level semiconductor ~~comprising~~ comprises a process to seal with a resin material the surface of wafer having the front surface and rear surface and forming a plurality of semiconductor

chips on ~~said~~ the front surface, a first marking process for marking the position information corresponding to each chip to the region of each chip at the rear surface of ~~said~~ the wafer, a process for performing the electrical test to each chip, a second marking process for marking the result of ~~said~~ the electrical test to the region of each chip at the rear surface of ~~said~~ the wafer and a dicing process for dicing the wafer to each chip.